IN THE CLAIMS:

Claims 1, 11, 19 and 20 are amended as follows:

Sub B1

A6

1. (Amended) A semiconductor integrated circuit device comprising:

a first power-on detection circuit responsive to a first power supply voltage for detecting power-on of said first power supply voltage to activate a first power-on detection signal according to a result of detection;

a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage to activate a second power-on detection signal according to a result of detection; and

a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals.

Sub B2

A7

11. (Amended) A semiconductor integrated circuit device comprising:

an internal voltage generation circuit receiving a first power supply voltage and generating, from said first power supply voltage, an internal voltage different in voltage level from said first power supply voltage;

an internal voltage application detection circuit for activating an internal voltage power-up detection signal according to a voltage level of said internal voltage;

a power-on detection circuit for detecting power-on of a second power supply voltage to activate a power-on detection signal according to a result of detection; and

a main power-on detection circuit responsive to said internal voltage power-up detection signal and said power-on detection signal for generating a main power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of internal voltage power-up detection signal and the power-on detection signal.

19. (Amended) A semiconductor device receiving a plurality of power supply voltages for operation, comprising:

a plurality of power-up detection circuits provided for the respective power supply voltages and detecting power-up of the respective power supply voltages to generate power-up detection signals corresponding to the respective power supply voltages; and

a main power-on detection circuit coupled to receive the power-up detection signals for activating a main power-up detection signal from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state.

20. (Amended) A semiconductor device comprising:

internal voltage generation circuitry coupled to receive at least one power supply voltage and generating, from said at least one power supply voltage, a plurality of internal voltage differing in voltage level from each other and from said at least one power supply voltage;

Concld A8

internal voltage power-up detection circuitry provided for at least one of the plurality of internal voltages and detecting power-up of the at least one internal voltage in accordance with a voltage level of said at least one internal voltage for generating at least one internal voltage power-up detection signal for said at least one internal voltage;

power-on detection circuitry provided for at least one power source voltage other than said at least one power supply voltage, for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage to generate at least one power-on detection signal for the respective at least one power source voltage; and

main power-on detection circuit responsive to said at least one internal voltage power-up detection signal and said at least one power-on detection signal for generating a main power-on detection signal made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state.